AMENDMENTS TO THE DRAWINGS

Attached hereto is one (1) sheet of corrected drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected drawings incorporate the following drawing changes:

In Figs. 1 and 2, the label "Related Art" has been added.

It is respectfully requested that the corrected drawings be approved and made a part of the record of the above-identified application.

REMARKS

Claims 1-20 are now present in this application.

Claims 1, 5 and 10 have been amended, and claims 15-20 have been presented. Reconsideration of the application, as amended, is respectfully requested.

Drawing Objection

The drawings stand objected to for certain informalities. Accordingly, attached hereto are replacement sheets for Figs. 1 and 2, in which the label "Related Art" has been added. Accordingly, reconsideration and withdrawal of any objection to the drawings are respectfully requested.

Amendments to the Claims

Various claims have been amended to particularly point out and distinctly claim the subject matter of the instant invention.

For example, line 19 of claim 1 and line 21 of the claim 4 have been amended to include the limitation ", wherein the first and second chips adhere to either surface of the same parts of the chip paddle". Support for this limitation can be found in Figs. 3 and 6 of the originally filed application. It is respectfully submitted that no new matter has been added.

Lines 13-15 of claim 10 have been amended to include the limitation "each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface". Further, lines 23-25 of claim 10 now recite "a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which ~~of~~

electrically connect with the second bonding pad and the wire connecting surface of the leads", and lines 29-32 of claim 10 recite "the total wire non-connecting surface of the leads exposed beyond the encapsulation". Support for these amendments can be found in page 7, lines 29-30, and Figs. 7 and 8 of the originally filed application. It is respectfully submitted that no new matter has been added.

Newly Presented Claims

Several claims have been presented to more clearly identify novels and non-obvious features of the claimed invention.

Independent claim 15 has been presented, which recites "the non-active surface of the first chip remains exposed when the outer leads are attached to an exterior device." Support for this limitation can be found on page 7, lines 9-27 and Fig. 8 of the originally filed application. Those skilled in the art would acknowledge that the device shown in Fig. 8 can be electrically connected to an exterior device such as a PCB by attachment of the outer leads 400b thereto. It is respectfully submitted that no new matter has been added.

New dependent claim 16 has been added, which recites "the wire non-connecting surface of the leads remains exposed when the outer leads are attached to an exterior device." Support for this limitation can be found on page 7, lines 9-27 and Fig. 8 of the originally filed application. Those skilled in the art would acknowledge that the device shown in Fig. 8 can be electrically connected to an exterior device such as a PCB by attachment of the outer leads 400b thereto. It is respectfully submitted that no new matter has been added.

New dependent claim 17 has been presented, which sets forth "the first and second chips adhere to either surface of the same parts of the chip paddle." Support for this limitation can be found in Figs. 7 and 8 of the originally filed application. It is respectfully submitted that no new matter has been added.

New dependent claim 18 has also been added, support for which can be found in Figs. 7 and 8 of the originally filed application. It is respectfully submitted that no new matter has been added.

New dependent claim 19 has been presented, which recites "the first and second chips adhere to either surface of the same parts of the chip paddle." Support for this limitation can be found in Figs. 7 and 8 of the originally filed application. It is respectfully submitted that no new matter has been added.

Rejection under 35 USC 102(e)

Claims 1-14 stand rejected under 35 USC 102(e) as being anticipated by SHIM et al., U.S. Publication 2004/0061202 A1. This rejection is respectfully traversed.

Claims 1 and 5

Claims 1 and 5 recite "the first and second chips adhere to either surface of the same parts of the chip paddle". This unique feature achieves a symmetrical packaging structure, effectively improving reliability. See Figs. 3 and 6-8, and page 8, lines 9-11 of the application.

SHIM et al. teaches that "the first and second chips adhere to different parts of the chip paddle". Specifically, SHIM et al. teaches that **the first chip 26** adheres to the **inner/center** chip

paddle 12 and **the second chip 30** adheres to the **outer ring** chip paddle 14 (see page 2, sections 0037 and 0041, for example). Figs. 1, 4, 5, 8-12 of SHIM et al. show that the packaging structures are not symmetrical due to the chip paddles are not symmetrical.

SHIM et al. does not teach or suggest that "the first and second chips adhere to either surface of the same parts of the chip paddle". Indeed, SHIM et al. teaches that **the first chip 26** adheres to the **inner/center** chip paddle 12 and **the second chip 30** adheres to the **outer ring** chip paddle 14. It is therefore respectfully submitted that claims 1 and 5 are allowable over the references utilized by the Examiner. Insofar as claims 2-4 and 6-9 depend from claims 1 and 5, it is respectfully submitted that these claims are also allowable.

Claim 10

Claim 10 recites that "**the non-active surface** of the **first chip** and the **total wire non-connecting surface of the leads** are **exposed** beyond the encapsulation." This unique feature improves heat dissipation, enhances reliability and reduces thickness of the packaging structure. See Figs. 7 and 8, page 7, line 30, and page 8, lines 1-5 of the application.

SHIM et al. teaches that "the non-active surface of the first chip is **covered** by a heat conductive layer" and "the wire non-connecting surface of the leads is partially **covered** by the encapsulant". Specifically, SHIM et al. teach the non-active surface of the first chip 126 is **covered** by a heat conductive layer 142, the wire non-connecting surface of the leads 116 is partially **covered** by the encapsulant 140, the non-active surface of **the first chip 226** is **covered** by a heat spreader 250, and the wire non-connecting surface of the leads 216 is partially **covered** by the encapsulant 240 (see Figs. 5 and 8, for example).

SHIM et al. does not teach or suggest that "the non-active surface of the first chip is **exposed** beyond the encapsulation" and "the wire non-connecting surface of the leads is partially **covered** by the encapsulant". Indeed, SHIM et al. teaches that **the first chips 126 and 226 are completely covered**, and the wire non-connecting surface of leads 116 and 216 are partially **covered** by the encapsulant 140 and 240. It is therefore respectfully submitted that claim 10 is allowable over the references utilized by the Examiner. Insofar as claims 11-18 depend from claims 10, it is respectfully submitted that these claims are also allowable.

Claim 15

Claim 15 recites that "the non-active surface of the first chip **remains exposed** when the outer leads are attached to an exterior device". This unique feature improves heat dissipation, enhances reliability and reduces thickness of the packaging structure. See Figs. 7 and 8, page 7, line 30, and page 8, lines 1-5 of the application.

SHIM et al. teaches that "the non-active surface of the first chip is **covered** by a heat conductive layer and an exterior device when the outer leads are attached to the exterior device" Specifically, SHIM et al. teaches that the non-active surface of the first chip 126 is **covered** by a heat conductive layer 142 and a motherboard (not shown) when the outer leads 118 are attached to the motherboard, and the first chip 226 is **covered** by a heat spreader 250 and a motherboard (not shown) when the outer leads 118 are attached to the motherboard (see sections 0050, 0058, 0059, and Figs. 5 and 8, for example).

SHIM et al. does not teach or suggest that "the non-active surface of the first chip **remains exposed** when the outer leads are attached to an exterior device". Indeed, SHIM et al.

teaches that the non-active surface of the first chips 126 and 226 are **covered** by a heat conductive layer 142, heat spreader 250, and a motherboard (not shown) when the outer leads 118 are attached to the motherboard. It is therefore respectfully submitted that claim 15 is allowable over the prior art utilized by the Examiner.

Claim 16

Claim 16 recites that "the wire non-connecting surface of the leads **remains exposed** when the outer leads are attached to an exterior device". This unique feature improves heat dissipation, enhances reliability and reduces thickness of the packaging structure. See Figs. 7 and 8, page 7, line 30, and page 8, lines 1-5 of the application.

SHIM et al. teaches that "the wire non-connecting surface of the leads is **covered** by an encapsulant when the outer leads are attached to the exterior device" Specifically, SHIM et al. teaches that the wire non-connecting surface of the lead portions 120 is **covered** by an encapsulant 140 when the outer leads 118 are attached to the motherboard, and the wire non-connecting surface of the lead portions 220 is **covered** by an encapsulant 240 when the outer leads 218 are attached to the motherboard (see sections 0050, 0058, 0059, and Figs. 5 and 8, for example).

SHIM et al. does not teach or suggest that "the wire non-connecting surface of the leads **remains exposed** when the outer leads are attached to an exterior device". Indeed, SHIM et al. teaches that the wire non-connecting surface of the lead portions 120 and 220 is **covered** by encapsulants 140 and 240 when the outer leads 118 and 218 are attached to the motherboard. It

is therefore respectfully submitted that claim 16 is allowable over the prior art utilized by the Examiner.

Claim 17

Claim 17 recites that "the first and second chips adhere to either surface of the same parts of the chip paddle". This unique feature achieves a symmetrical packaging structure, effectively improving reliability. See Figs. 3 and 6-8 and page 8, lines 9-11 of the application.

SHIM et al. teaches that "the first and second chips adhere to different parts of the chip paddle". Specifically, SHIM et al. teaches that **the first chip 26** adheres to the **inner/center** chip paddle 12 and **the second chip 30** adheres to the **outer ring** chip paddle 14. See page 2, sections 0037 and 0041, for example. Figs. 1, 4, 5 and 8-12 of SHIM et al. show that the packaging structures are not symmetrical due to the chip paddles not being symmetrical.

SHIM et al. does not teach or suggest that "the first and second chips adhere to either surface of the same parts of the chip paddle". Indeed, SHIM et al. teaches that **the first chip 26** adheres to the **inner/center** chip paddle 12 and **the second chip 30** adheres to the **outer ring** chip paddle 14. It is therefore respectfully submitted that claim 17 is allowable over the prior art utilized by the Examiner.

Claim 18

Claim 18 recites that "the **total wire non-connecting surface of the leads** are **exposed** beyond the encapsulation". This unique feature improves heat dissipation, enhances reliability

and reduces thickness of the packaging structure. See Figs. 7 and 8, page 7, line 30, and page 8, lines 1-5 of the application.

SHIM et al. teaches that "the wire non-connecting surface of the leads is partially **covered** by the encapsulant". Specifically, SHIM et al. teaches that the wire non-connecting surface of the leads 116 is partially **covered** by the encapsulant 140, and the wire non-connecting surface of the leads 216 is partially **covered** by the encapsulant 240 (see Figs. 5 and 8, for example).

SHIM et al. does not teach or suggest that "the wire non-connecting surface of the leads is partially **covered** by the encapsulant". Indeed, SHIM et al. teaches that the wire non-connecting surface of leads 116 and 216 are partially **covered** by the encapsulant 140 and 240. It is therefore respectfully submitted that claim 18 is allowable over the prior art utilized by the Examiner. Insofar as claim 19 depends from claims 18, it is respectfully submitted that this claim is also allowable.

Claim 19

Claim 19 recites that "the first and second chips adhere to either surface of the same parts of the chip paddle". This unique feature achieves a symmetrical packaging structure, effectively improving reliability. See Figs. 3 and 6-8 and page 8, lines 9-11 of the application.

SHIM et al. teaches that "the first and second chips adhere to different parts of the chip paddle". Specifically, SHIM et al. teaches that **the first chip 26** adheres to the **inner/center** chip paddle 12 and **the second chip 30** adheres to the **outer ring** chip paddle 14. See page 2, sections

0037 and 0041, for example. Figs. 1, 4, 5, 8-12 of SHIM et al. show that the packaging structures are not symmetrical due to the chip paddles not being symmetrical.

SHIM et al. does not teach or suggest that "the first and second chips adhere to either surface of the same parts of the chip paddle". Indeed, SHIM et al. teaches that **the first chip 26** adheres to the **inner/center** chip paddle 12 and **the second chip 30** adheres to the **outer ring** chip paddle 14. It is therefore respectfully submitted that claim 19 is allowable over the prior art utilized by the Examiner.

Claim 20

Claim 20 recites that "the wire non-connecting surface of the leads **remains exposed** when the outer leads are attached to an exterior device". This unique feature improves heat dissipation, enhances reliability and reduces thickness of the packaging structure. See Figs. 7 and 8, page 7, line 30, and page 8, lines 1-5 of the application.

SHIM et al. teaches that "the wire non-connecting surface of the leads is **covered** by an encapsulant when the outer leads are attached to the exterior device" Specifically, SHIM et al. teaches that the wire non-connecting surface of the lead portions 120 is **covered** by an encapsulant 140 when the outer leads 118 are attached to the motherboard, and the wire non-connecting surface of the lead portions 220 is **covered** by an encapsulant 240 when the outer leads 218 are attached to the motherboard (see sections 0050, 0058, 0059, and Figs. 5 and 8, for example).

SHIM et al. does not teach or suggest that "the wire non-connecting surface of the leads **remains exposed** when the outer leads are attached to an exterior device". Indeed, SHIM et al.

teaches that the wire non-connecting surface of the lead portions 120 and 220 is **covered** by encapsulants 140 and 240 when the outer leads 118 and 218 are attached to the motherboard. It is therefore respectfully submitted that claim 20 is allowable over the prior art utilized by the Examiner.

Conclusion

In view of foregoing amendments and remarks, it is respectfully submitted that prior art utilized by the Examiner fails to teach or suggest the dual chips stacked packaging structures of the present application. Accordingly, reconsideration and withdrawal of the 35 USC 102(e) rejection are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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